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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,787	03/22/2004	Prashant Sethi	42P18870	2369

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
LEE, CHUN KUAN	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,787	SETHI ET AL.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/22/2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Fritz M. Fleming

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
7/24/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/27/05 & 6/8/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because Figure 3 appears unclear as to what the lines, dashed-lines and letters, on the upper right part of the page, is showing. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4, 10, 13, 16 and 20 contain the trademark/trade name "PCI Express". Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods

associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe PCI type interconnection and, accordingly, the identification/description is indefinite.

3. Claims 3, 8 and 10 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3 and 8 recite the limitation "wherein the network fabric" in page 9, line 15 and page 10, line 14, respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 recites the limitation "wherein the PCI type interconnection" in page 10, line 16. There is insufficient antecedent basis for this limitation in the claim.

As per claims 3 and 8, it appears unclear as to which "network fabric" the applicant is referring to, as the independent claims 1 and 6, which claims 3 and 8 are dependent on respectively, does not recite the limitation of a network fabric. Examiner will assume claim 3 is dependent on claim 2 and claim 8 is dependent on claim 7 for the current examination.

As per claim 10, it appears unclear as to which "PCI type interconnection" the applicant is referring to, as the independent claim 6, which claim 10 is dependent on, does not recite the limitation of a PCI type interconnection. Examiner will assume that claim 10 is dependent on claim 9 for the current examination.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-11 and 18-21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

5. As per claim 1, the independent method claims comprises the decoding step, the routing step and the forwarding step, wherein the plurality of steps does not appear to produce a tangible result.

6. As per claims 6 and 21, each of the respective independent method claims comprises the decoding step and the routing step, wherein the plurality of steps does not appear to produce a tangible result.

7. As per claims 2-5 and 7-11, each of the respective dependent method claims, dependent on the independent claims 1 and 6, does not appear to include limitation that may fix the deficiency associated with independent claims 1 and 6, therefore claims 2-5 and 7-11 are rejected at least due to dependency on the independent claims 1 and 6.

8. As per claims 18-20, the claimed subject matter comprises a machine-readable medium, wherein it is defined in the specification, on page 6 lines 25-26, that the

machine-readable medium may be a form of propagated signal and signal is non-statutory subject matter.

Claim Rejections - 35 USC § 102

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

9. Claims 1, 4, 6, 9-10, 12-13, 15-16, 18 and 20 are rejected under 35 U.S.C. 102(a) as being anticipated by "BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors".

10. As per claim 1, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches a method for configuring an integrated device (e.g. memory controller) in a first processor (e.g. processor node or application processor (AP)) (Section 2.1 on page 21 and Section 2.1.4 on page 23) comprising:

decoding (decoding by initialization) a memory configuration access within a second processor (e.g. bootstrap processor (BSP)) (Section 2.1 on page 21 and Section 2.1.4 on page 23),

the second processor coupled to the first processor, to a configuration cycle (Section 3.1 on page 25);

routing the configuration cycle to a chipset (e.g. host bridge) based at least in part on a routing information (Section 2.1.1 on pages 21-22; Section 3.1 on page 25 and Chapter 8 on page 203); and

forwarding the configuration cycle (Section 2.1.4 on page 23).

11. As per claim 4, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches the method comprising wherein the chipset has a bridge (e.g. host bridge) and adheres to a PCI type interconnect that is either PCI or PCI Express (Section 2.1.1 on pages 21-22 and Section 3.1 on page 25).

12. As per claim 6, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches a method for configuring an integrated device (e.g. circuitry utilized for the address map table) in a first processor (e.g. processor node or application processor (AP)) (Section 2.1 on page 21 and Section 2.1.5 on page 23) comprising:

decoding (decoding by initialization) an Input Output (IO) configuration access within a second processor (e.g. bootstrap processor (BSP)), coupled to a first processor, to a configuration cycle (Section 2.1 on page 21 and Section 2.1.5 on page 23); and

routing the configuration cycle to the integrated device based at least in part on a routing information (Section 2.1.1 on pages 21-22; Section 3.1 on page 25 and Chapter 8 on page 203).

13. Claims 9-10 repeat the limitations of claim 4 and are therefore rejected accordingly.

14. As per claims 12, 15 and 18, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches a system and an article of manufacture comprising a machine readable medium comprising:

a first processor (e.g. bootstrap processor (BSP)) with an decoder coupled to a second network component (e.g. processor node or application processor (AP)) with an integrated device (Section 2.1 on pages 21 and Section 3.1 on page 25), wherein BSP is responsible for the initialization process, therefore must have the necessary decoder to implement the initialization process;

the decoder to decode (decode by initiation) either a memory or IO configuration access to a configuration cycle (Section 2.1 on page 21; Section 2.1.4-2.1.5 on page 23 and Section 3.1 on page 25); and

to transmit (transmit by routing) the configuration cycle to either a chipset (e.g. host bridge) or integrated device, wherein the configuration cycle adheres to a PCI type interconnect (Section 2.1.1 on pages 21-22; Section 3.1 on page 25 and Chapter 8 on page 203).

15. Claims 13, 16 and 20 repeat the limitations of claim 4 and are therefore rejected accordingly.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 2-3, 5, 7-8, 11, 14, 17, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over "BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors" in view of "HyperTransport™ Technology I/O Link".

17. As per claims 2-3, 5, 7-8, 11, 14, 17 and 19, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches all the limitations of claim 1 as discussed above, where BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors further teaches the method comprising the utilization of HyperTransport Links (Section 2.1.1 on page 21-22) and the configuration cycle is routed to the chipset (e.g. host bridge) (Section 3.1 on page 25).

BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors does not expressly teaches the method comprising:

wherein the configuration cycle is routed to the chipset via a network fabric;

wherein the network fabric is a plurality of point to point links;

wherein the second processor is coupled to the first processor via the network fabric; and

wherein the chipset or integrated device is coupled to the decoder via a network fabric.

HyperTransport™ Technology I/O Link teaches the system and method comprising a networking of a plurality of processor (Fig. 10 on page 20), wherein the

networking comprises a point-to-point link ("The HyperTransport™ Technology Solution" Section on page 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include HyperTransport™ Technology I/O Link's networking and point-to-point link into BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors' method. The resulting combination of the references teaches the method further comprising:

wherein the configuration cycle is routed to the chipset through the network interconnection;

wherein the network interconnection comprises the plurality of point-to-point links;

wherein the second processor is coupled to the first processor through the network interconnection; and

wherein the host bridge is coupled to the decoder via the network interconnection.

Therefore, it would have been obvious to combine HyperTransport™ Technology I/O Link with BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors in order to conform to the standard set forth by the HyperTransport™ I/O Link Specification as BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors utilized the plurality of HyperTransport links.

18. As per claim 21, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches a method for configuring an integrated device (e.g. memory controller) in a first processor (e.g. processor node or application processor (AP)) (Section 2.1 on page 21 and Section 2.1.4 on page 23) comprising:

decoding (decoding by initialization) a memory configuration access within a second processor (e.g. bootstrap processor (BSP)) (Section 2.1 on page 21 and Section 2.1.4 on page 23),

the second processor coupled to the first processor, to a configuration cycle (Section 3.1 on page 25); and

routing the configuration cycle to the first processor (Section 2.1.1 on pages 21-22; Section 3.1 on page 25 and Chapter 8 on page 203).

BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors does not expressly teach the method comprising wherein routing the configuration cycle from a chipset to the first processor via a bridge.

HyperTransport™ Technology I/O Link teaches the system and method comprising a multiple chain of tunnel devices connected to a bridge, which is then connected to a host bridge ("Device Configuration" section on page 7).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include HyperTransport™ Technology I/O Link's interconnection utilizing the host bridge and bridge into BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors' method. The resulting combination of the

references teaches the method further comprising the routing of the configuration cycle from the host bridge (chipset) to the bridge then to the first processor.

Therefore, it would have been obvious to combine BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors and HyperTransport™ Technology I/O Link for reason stated above in claims 2-3, 5, 7-8, 11, 14, 17 and 19.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ftzm. Fleming

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
7/24/2006

C.K.L.
07/20/2006